## REMARKS

Prior to entry of this paper, claims 1, 3-16, 18, 19, 21, 22, 24, and 26-30 were pending. Claims 1, 3-13, 15, 18, 21, 22, 24, and 28-30 were rejected. Claims 14, 16, 19, 26, and 27 were objected to, but were identified as being allowable if re-written in independent form. In this paper, Claims 1-30 are cancelled, and new Claims 31-59 are added. No new matter is added by way of this amendment. Claims 31-59 are currently pending.

Claims 31-59 are identical to Claims 1-29 respectively as they stood after entry the amendment submitted by Applicants on 4/25/05 (but prior to entry of the amendment filed on 7/27/05). The correspondence between the current claims and the original claim numbering may be obtained by simply subtracting 30 from the current claim numbers. This amendment was made to restore Claims 1-29 to their earlier form prior to entry of the amendment filed on 7/27/05, since the amendment filed on 7/27/05 was only made due to the fact that the last Office Action had been made final. Since the finality of the Office Action has been withdrawn, Applicants restore the claims to their previous state by canceling the claims and re-writing them in their previous form.

For at least the following reasons, Applicants respectfully submit that each of the presently pending claims is in condition for allowance.

## Allowable Subject Matter (Claims 44-46, 49, 56, and 57)

Claims 14, 16, 19, 26, and 27 were objected to as being dependent on a rejected base claim, but were identified as being allowable if rewritten in independent form. Claims 44, 46, 49, 56, and 57 are simply re-numbered versions of Claims 14, 16, 19, 26, and 27, respectively. Claim 45 depends on Claim 44. Accordingly, Claims 44-46, 49, 56, and 57 contain subject matter identified by the Examiner as being allowable.

It is respectfully submitted that the base claims are allowable for at least the reasons stated below. Accordingly, it is respectfully submitted that Claims 44-46, 49, 56, and 57 are in condition for allowance.

**Claims 31-36, 38-43, 47, 48, 50-54, 58, and 59**

It is respectfully submitted that Claim 31 is allowable at least because neither Yamauchi (U.S. Patent 6,356,141) nor Macaluso I (U.S. Patent 6,380,797) nor Macaluso II (U.S. Patent 6,600,346) discloses, "a feedback circuit that is coupled to the first and second variable resistance circuits, wherein a source resistance of the output driver circuit appears to a load as substantially similar to a termination resistance of the load", as recited in Applicants' Claim 31. Further, it is respectfully submitted that the rejection to Claim 33 should be withdrawn at least because neither Yamauchi nor Macaluso I nor Macaluso II discloses "the feedback circuit is configured to adjust the first variable resistance circuit and the second variable resistance circuit to track a change in the termination resistance, such that the source resistance tracks the change in the termination resistance", as recited in Applicants' Claim 33.

The Office Actions have stated that feedback circuit 30 of Fig. 1 of Yamauchi inherently meets the limitations quoted in the above paragraph. Applicants respectfully disagree. As stated in declaration 8 of Declaration of Ivan Duzevik Under C.F.R. § 1.132 (Duzevik), "Gate voltage control circuit 30 of Fig. 1 of Yamauchi does not affect the source resistance of the output driver circuit (as seen from the output terminals)."

Similarly, the Office Actions have stated that the limitations of Claims 31 and 33 recited above are inherently performed by the circuit of FIG. 2 of Macaluso I. Applicants respectfully disagree. As stated in declaration 11 of Duzevik, "In FIG. 2 of Macaluso I, the source resistance as seen by the output terminals does not track the termination resistance."

Similarly, the Office Actions have stated that the limitations of Claims 31 and 33 recited above are inherently performed by the circuit of FIG. 2 of Macaluso II. Applicants respectfully disagree. As stated in declaration 13 of Duzevik, "In FIG. 2 of Macaluso II, the source resistance as seen by the output terminals does not track the termination resistance."

Further, Claim 36 is respectfully submitted to be allowable at least because neither Yamauchi nor Macaluso I nor Macaluso II discloses, "the feedback circuit is configured to adjust an on-resistance that is associated with the transistor", as recited in Applicants' Claim 36. As is well known in the art, a MOSFET biased in the linear region of operation behaves approximately like a resistor having an on-resistance that is approximately inversely proportional to $V_{GS}$-$V_T$. However,

in the saturation region, rather than behaving like a resistor, a MOSFET provides a drain current that is approximately proportional to $(V_{GS}-V_T)^2$, and behaves approximately as a current source or current sink rather than as a resistor. Because transistors 11 and 14 of Yamauchi and transistors M84 and M94 of Macaluso I and transistors M9 and M10 of Macaluso II are biased in saturation mode rather than linear mode, the feedback does not "adjust an on-resistance that is associated with the transistor."

Further, Claim 51 is respectfully submitted to be allowable at least because neither Yamauchi nor Macaluso I nor Macaluso II disclose, "the feedback circuit is arranged to, if the feedback circuit is enabled, bias the transistor such that the transistor operates in a linear region of operation." Transistors 11 and 14 of Yamauchi; transistors M84 and M94 of Macaluso I; and transistors M9, M10, M6, and M8 of Macaluso II are biased in saturation mode rather than the linear mode (see Duzevik declarations 9, 10, 12, and 14).

Further, it is respectfully submitted that the rejection should be withdrawn with regard to Claims 47 and 50 at least for reasons similar to those stated above with regard to Claim 31. Further, it is respectfully submitted that the rejection should be withdrawn with regard to Claims 32-33, 35, 36 , and 51 at least because they depend from Claim 31, which is proposed to be allowable. Claims 48 and 52 are respectfully submitted to be allowable at least because it depends on Claim 45, which is proposed to be allowable. Claim 53 is respectfully submitted to be allowable at least because it depends on Claim 50, which is proposed to be allowable.

**Rejections under 35 U.S.C. § 103(a) (Claims 37 and 55)**

Claims 7-13, 24, and 28-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamauchi* in view of any one of *Raymond*, *Nagano et al.*, and *Cho et al.* Claim 7 is now pending as Claim 37 in this paper; accordingly, the rejection under 35 U.S.C. § 103(a) would stand with regard to Claim 37, and to Claim 55 (Claim 55 is substantially the same as Claim 24 as Claim 24 stood prior to entry of the amendment filed on 7/27/05). The rejection under 35 U.S.C. § 103 (a) is respectfully traversed.

Applicants note that a reference named "*Cho et al.*" has not been identified by patent number or other means of identifying what reference is being referred to, and no such reference has

been cited at any point. Accordingly, Applicants ignore "Cho et al" and assume that the rejected claims are deemed unpatentable over *Yamauchi* in view of any one of *Raymond* or *Nagano et al.*

The rejection under 35 U.S.C. § 103(a) is respectfully traversed at least because a prima facia case of obviousness has not been made. It is respectfully submitted that there is no motivation modify Yamauchi by placing a resistor in parallel with either transistor 11 or transistor 14 of Yamauchi. Transistor 11 of Yamauchi is a current source, and transistor 14 is a current sink. None of the cited references provide any motivation to place a resistor in parallel with a current sink or a current source.

In column 3, lines 7-15, Romano describes that a fixed resistor 56 may be placed in parallel with a controlled variable resistor element, such as a FET acting as a linear voltage variable resistor. Nothing in Romano suggest placing a fixed resistor in parallel with a current source or a current sink. The Office Action states the motivation would be "to obtain the various advantages associated with such a parallel arrangement, see column 3, lines 8-15 of Raymond." However, the advantage cited at column 3, lines 8-15 of Raymond would not be applicable to placing a resistor in parallel with transistor 11 or transistor 14 of Yamauchi.

The same is true for Raymond. In FIG. 9 of Raymond, N channel transistors 33, 34, 53, and 54 are connected in parallel to the resistors 35, 36, 55, and 56 respectively. However, nothing in the Raymond reference suggests the desirability of placing a resistor in parallel with a current source or a current sink. FIG. 9 of Raymond does include a current source 41 and a current sink 42. Raymond does not suggest placing a resistor in parallel with either current source 41 or current sink 42.

Although a Cho reference has not been identified, presumably, the same statements as above would apply to the Cho reference, if there is such a reference. That is, if there is a Cho reference, Applicants presume that nothing in the Cho reference suggests the desirability of placing a resistor in parallel with either a current sink or a current source. Most likely, the Cho reference, if there is one, shows a resistor in parallel with a FET in a linear region of operation such as described in Romano as discussed above.

## CONCLUSION

It is respectfully submitted that each of the presently pending claims (Claims 31-59) are in condition for allowance and notification to that effect is requested. Examiner is invited to contact the Applicants' representative at the below-listed telephone number if it is believed that the prosecution of this application may be assisted thereby. Although only certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentable. Applicant reserves the right to raise these arguments in the future.

Dated: November 22, 2005

Respectfully submitted,

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